Thermal Studies of Individual Si/Ge Heterojunctions — The Influence of the Alloy Layer on the Heterojunction

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(Submitted on June 15, 2019)

Abstract

Phonon transport across an interface is of fundamental importance to applications ranging from electronic and optical devices to thermoelectric materials. Examples of such interfaces include grain boundaries within a polycrystalline material or heterostructure interfaces within a nanocomposite or devices built with film-wafer bonding. The phonon scattering by an interface can dramatically suppress the thermal transport, which can benefit thermoelectric applications but create problems for the thermal management of electronic/optical devices. In this aspect, numerous molecular dynamics simulations on phonon transport across various interfaces are often based on guesstimates of atomic structures and are seldom compared with measurements on real interfaces. In this work, planar Si/Ge heterojunctions formed by film-wafer bonding are measured for the interfacial thermal resistance to compared with predictions by existing simulations and analytical models. Different twist angles between a 70-nm-thick Si film and a Ge wafer are used to check the influence of the crystal misorientation. Detailed transmission electron microscopy studies are carried out to better understand the interfacial atomic structure. It is found that the thermal resistance of the alloyed interfacial layer with mixed Si and Ge atoms is dominant for the measured . Following this, reduction should be focused on how to minimize the interdiffusion of Si and Ge atoms during the formation of a Si/Ge heterojunction.

**1. Introduction**

For many engineering applications, phonon transport across an interface has remained as one central topic for research on nanoscale heat transfer [[1](#_ENREF_1), [2](#_ENREF_2)]. In physics, the phonon reflection and transmission by an interface can introduce an interfacial thermal resistance *RK*, known as the Kapitza resistance [[3-5](#_ENREF_3)]. However, the exact interaction between an interface and incident phonons is still not well understood even after decades of research. In the widely used acoustic mismatch model (AMM) and diffuse mismatch model (DMM), an interface is viewed as a plane to join two materials and the bulk phonon properties of both materials are used to compute the phonon transmissivity and thus *RK*. The intrinsic properties of an interface are not considered though a real interface can be a complicated layer region with disorder, roughness, dislocation, and often atom intermixing [[6](#_ENREF_6)]. In the extended DMM, an interfacial layer is viewed as a third medium with its unique properties [[7](#_ENREF_7)]. In more advanced studies, the interactions between a phonon and an interface can be extracted from molecular dynamics (MD) simulations [[8-11](#_ENREF_8)] and the atomistic Green’s function (AGF) approach [[12-15](#_ENREF_12)]. By merging lattice dynamics methods with MD simulations, a new formalism termed interface conductance modal analysis was also used to study interfacial phonon transport [[16](#_ENREF_16)]. However, the assumed interfacial structures are usually oversimplified and direct comparison to measurements are mostly restricted to deposited layered thin films with high-quality interfaces. In contrast, more defects are usually found on the nanosized interfaces within a material synthesized by hot pressing nanopowder into the bulk form. Particularly for heterojunctions, interdiffusion of different atoms during the high-temperature material synthesis can introduce an alloy layer to largely restrict the phonon transport. Such an interfacial layer was neglected in many studies on Si/Ge heterojunctions [[11](#_ENREF_11), [17](#_ENREF_17)] but was recognized in one recent study [[15](#_ENREF_15)].

Experimentally, it is still challenging to measure a single interface within a bulk material. As a simpler approach, bonding between two rigid wafers has been used to represent a twist grain boundary for thermal studies [[18](#_ENREF_18), [19](#_ENREF_19)]. However, the interfacial thermal stress introduced during the bonding process can largely affect the quality of the formed interface, which becomes more critical for two different materials such as Si and Ge. This problem can be solved by bonding a super-flexible thin film onto a rigid wafer. In this case, the thermal-mismatch strain energy is almost all stored inside the film and the total stored energy is proportional to the small film thickness. The flexible thin film also ensures good adhesion between the film and rigid wafer to ensure good contact for bonding formation. Along this line, extremely high-quality bonding has been demonstrated between a 200-nm-thick and millimeter-sized Si membrane and a Ge wafer, with thin ~1.2 nm region for the bonded Si-Ge interface as revealed by transmission electron microscopy (TEM) studies [[20](#_ENREF_20)].

In this work, the high-quality bonded interface between a 70-nm-thick (100) Si film and a (100) Ge wafer was used to study the formation and the resulting *RK* for the corresponding heterojunction. Different twist angles between the Si film and the Ge wafer were used to check the impact of misorientations on *RK.* The experimental data were directly compared to existing simulations. Systematic TEM studies were carried out to better understand the complicated interfacial atomic structure, particularly the SiGe alloy layer at the interface. The studied Si/Ge heterojunctions were widely used in high-performance photodiodes [[21](#_ENREF_21), [22](#_ENREF_22)], thermoelectric nanocomposites [[23](#_ENREF_23), [24](#_ENREF_24)], superlattice nanowires and thin films [[25](#_ENREF_25), [26](#_ENREF_26)]. Unrestricted to Si/Ge interfaces, *RK* studies of film-wafer bonding are also critical to many applications that use film-wafer bonding for microdevice fabrication and thermal management of power devices, e.g., GaN-diamond bonding for better heat dissipation [[27](#_ENREF_27)].

**2. Experimental**

*2.1 Film-wafer bonding*

The employed 70-nm-thick Si film was released as the device layer from a commercial silicon-on-insulator (SOI) wafer. Strips with the width of 400 µm were defined using photolithography. Then the unprotected part of the Si thin film was etched using reactive ion etch while the thin film to be transferred were under protection of the photoresist. The Si film was released by etching off the buried SiO2 layer on a SOI wafer with hydrofluoric acid (HF). With the photoresist as the protection layer, the film transfer process was similar to those widely used for two-dimensional materials [[28](#_ENREF_28)]. As an alternative way, a thermal release tape may also be used for the film transfer process [[20](#_ENREF_20)]. The photoresist or residue from the thermal release tape was removed with acetone and then isopropyl alcohol (IPA). On the other side, the Ge substrates were cleaned by sonication in acetone, IPA and deionized (DI) water for 15 minutes each. The Ge substrate were further cleaned by HF:HCl:H2O (1:1:10) solution for 20 minutes [[20](#_ENREF_20)]. HF should leave an oxygen free surface and HCl should leave a carbon free surface. In the final step, Ge substrates were risen under DI water for 10 minutes to remove the HF/HCl residue on the Ge surface.

The Si/Ge bonding was formed by annealing the samples at 673 K for 30 minutes in a tube furnace with nitrogen flow, following the previous work on Si/Ge bonding [[20](#_ENREF_20)]. The temperature was ramped up slowly at the rate of 5K/min to minimize any damages due to the mismatch between the thermal expansion coefficients of Si and Ge. The same 5K/min rate was used during the cool down process. Figure 1a shows the scanning electron microscopy (SEM) image of a 70-nm-thick Si film bonded onto a Ge substrate. Using an atomic force microscope (AFM), the surface undulation across the Si film was mostly <1 nm over a 5 μm ×5 μm region after thermal bonding (Fig. 1b).

In the synthesis of bulk SiGe nanocomposites, a pressure was typically applied in a typical hot press process [[29](#_ENREF_29), [30](#_ENREF_30)]. However, it was found that adding a moderate ~50 MPa pressure during the bonding process may cause wrinkles on the relatively soft Ge substrate. Therefore, thermal bonding for typical device fabrications was employed here and no pressure was applied.

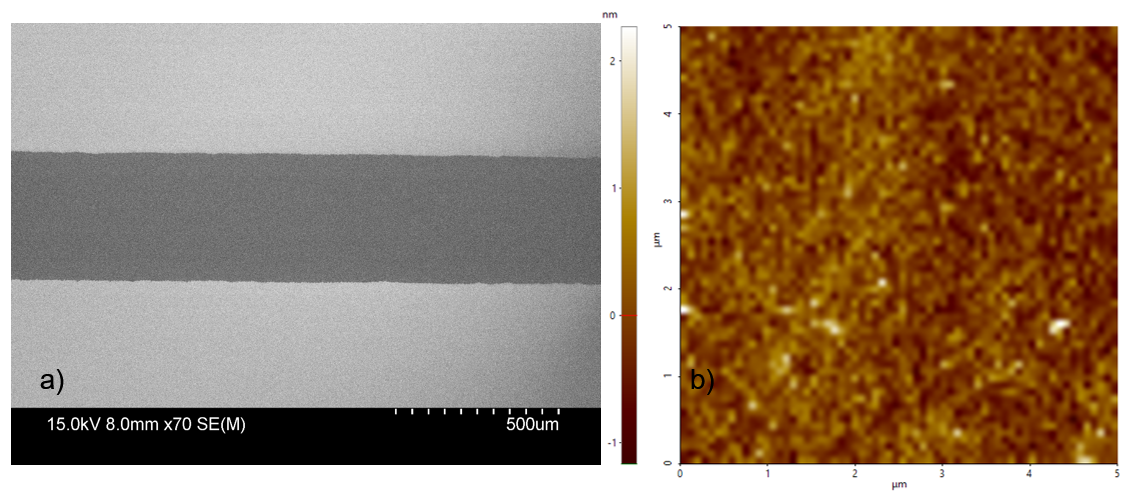


Figure 1 (a) SEM image of a Si film on a Ge wafer. (b) Surface undulation of a Si film bonded onto a Ge substrate.

*2.2 Thermal characterization*

For measurements, an 80-nm-thick Al2O3 layer was deposited across the whole wafer for electrical insulation. On the Ge substrate, the region without the bonded Si film was used as the reference. For measured regions, 20-nm-thick Cr and then 200-nm-thick Au were deposited as a metal-line heater/thermometer (Fig. 2 inset). The metal line was 20 µm wide and 3.5 mm long, ensuring one-dimensional heat conduction through the 70 nm film thickness.

An offset 3*ω* technique [[31](#_ENREF_31), [32](#_ENREF_32)] was used to measure the summation of the cross-plane thermal resistances for the Si film () and the Si/Ge interfacial . Neglecting the difference in the values for the Al2O3/Si and Al2O3/Ge interfaces, can be extracted from the in-phase ac temperature oscillation Δ*TAC* curves for a film-wafer assembly and its reference on the same Ge wafer (Fig. 2). In the linear regime, these two Δ*TAC* curves are shifted by a constant value, . Here and are the amplitude of the heating power at the 2*ω* frequency and area of the metal line, respectively.

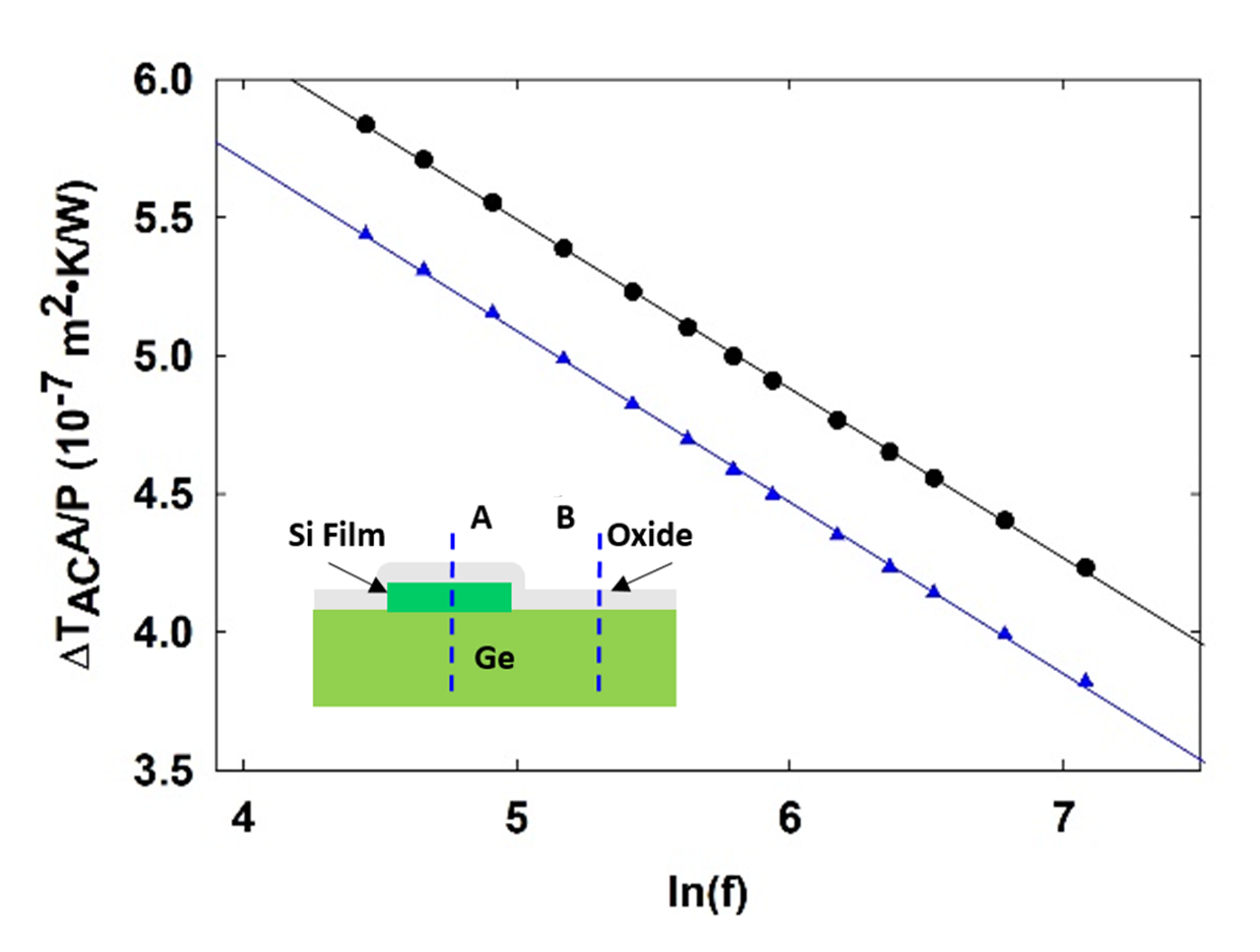


Figure 2. for an offset 3*ω* test, with the inset showing the cross-section diagram of the measurement setup. Usually 13 frequencies are selected for each sample (symbols) and the linear fitting of the data shows R2>0.9998. The black curve and circles are for location A, with Al2O3-coated film-wafer assembly. The blue curve and triangles are for reference location B, without the Si film. The shift between the two curves is per unit area.

Detailed uncertainty analysis of similar film-wafer measurements can be found in our previous work [[33](#_ENREF_33)]. In data analysis, is extracted by averaging the shift over all frequencies in Fig. 2. For this averaged , the half width of its 95% confidence interval () ranges from 1.8×10-10 to 2.4×10-9 m2·K/W for all temperature-dependent measurements, which is 0.19−2.4% divergence of the extracted value. The second error source can be the thickness variation of the deposited Al2O3 layer on the film-wafer assembly and at the reference location on the same Ge wafer. This thickness variation was within 0.5 nm, as checked with spectroscopic reflectometry (Filmetrics F-20). In the literature, the cross-plane thermal conductivity of a similar Al2O3 layer was measured at different temperatures [[34](#_ENREF_34)]. This thickness variation corresponds to an uncertainty that is 8.3×10-10 m2·K/W at 77 K and decreases to 3.1×10-10 m2·K/W at 300 K. The overall uncertainty is computed as for extracted .

**3. Results and Discussion**

*3.1 Cross-plane RFilm calculation*

Because the offset 3*ω* technique cannot separate and , the required cross-plane is calculated using the film thickness =70 nm and bulk phonon MFP , the latter of which depends on the phonon branch and phonon angular frequency . The effective phonon MFP, , is expressed as [[35](#_ENREF_35)]. This effective phonon MFP is then input into the kinetic relationship, i.e., , where is the differential phonon specific heat per unit volume and is the phonon group velocity. At 300 K, the employed bulk phonon MFPs are computed by Esfarjani *et al.* [[36](#_ENREF_36)]. Below 300 K, the temperature dependence of is taken into account by a factor , i.e., [[37](#_ENREF_37)]. The Debye temperature is =645 K in . The details of this calculation can be found in our previous work [[33](#_ENREF_33)]. Using the computed cross-plane , the required is plotted in Fig. 3 and used in the data analysis. This is less than 8% of the extracted at 300 K and decreases to 1.5% of the extracted at 83 K.

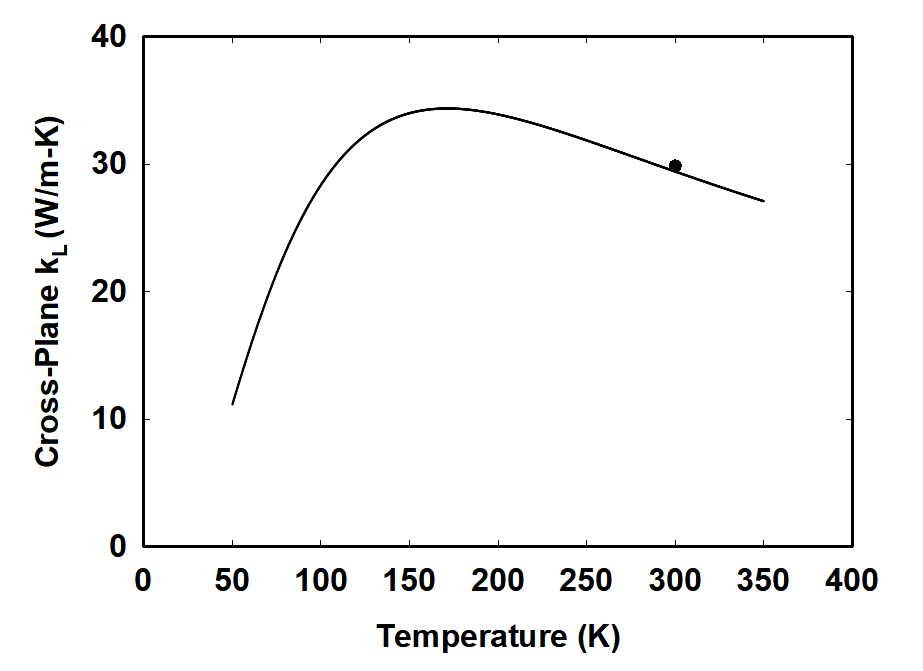


Figure 3. Temperature-dependent cross-plane computed for a 70-nm-thick Si film. The black dot is from a separated calculation by Jeong et al. [[38](#_ENREF_38)].

*3.2 TEM studies of the interfacial atomic structure*

Figures 4a and 4b show the interfacial atomic structures of two representative samples with twist angles of 1.1˚ and 12.6˚ between the Si film and Ge wafer, respectively. For TEM studies, both samples are cut from the film-wafer assembly with a focused ion beam (FIB) and then transferred onto a TEM grid. An interfacial layer (or interlayer) of around 2.6–2.8 nm thickness can be observed at the Si/Ge interface. The sample with a 12.6˚ twist angle has a slightly thicker interface. The observed interlayer thickness is comparable to the ~2 nm thickness for bonding formed between a Si wafer and a Ge wafer below 673 K [[22](#_ENREF_22)], and the ~3 nm thickness for room-temperature bonding between Si and Ge ribbons [[39](#_ENREF_39)]. Additional 673 K annealing for 30 minutes in N2 can increase the interlayer thickness to 3.5 nm for ribbon bonding [[39](#_ENREF_39)]. In the literature, a slightly thinner ~1.2 nm interlayer has also been observed for the bonding between a Si film and a Ge wafer at 673 K [[20](#_ENREF_20)]. The divergence between various studies can be attributed to the slightly stronger/weaker surface oxidation on the Ge wafer before the thermal bonding [[39](#_ENREF_39), [40](#_ENREF_40)].

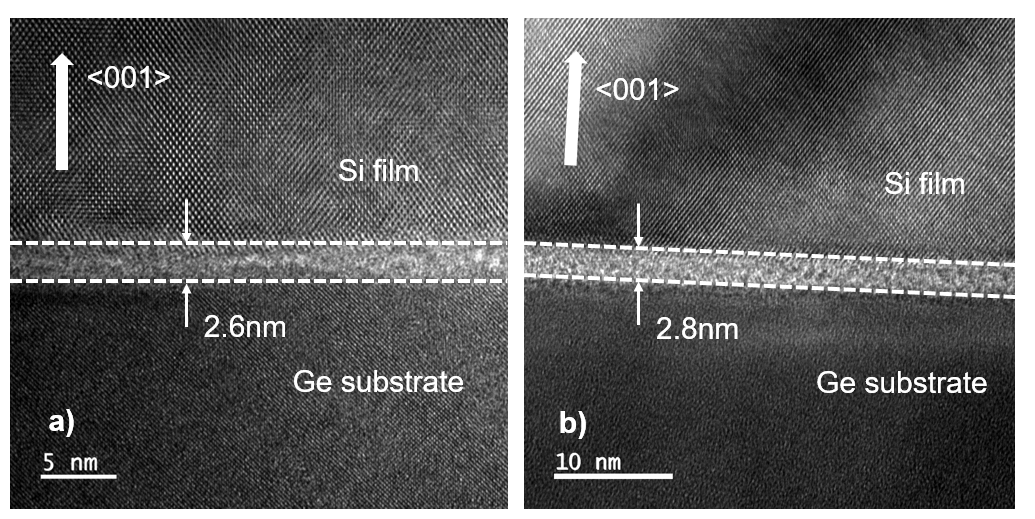


Figure 4. Cross-sectional TEM images of film-wafer interfaces with a twist angle of (a) 1.1˚ and (b) 12.6˚. The interface region is enclosed by dashed lines, with the thickness indicated.

Energy-dispersive X-ray spectroscopy (EDS) is conducted to further study the elemental composition across the interface. Similar results have been observed for the two samples with 1.1˚ and 12.6˚ twist angles so that only the 12.6˚ sample is presented here. The element mapping (Fig. 5a) reveals that the interface region mainly consists of Si, Ge and O. An almost uniform C percentage of 2%–3% is observed for the whole cross section, which can be attributed to the C contamination within the FIB chamber. In the literature, C contamination at the bonded Si/Ge interface has been reported before [[39](#_ENREF_39), [41](#_ENREF_41)] and has been suspected as the result of the residue from the thermal release tape [[39](#_ENREF_39)]. However, the C contamination is not found in the current study, in which a thermal release tape is not used. Other than Si and Ge, the higher O concentration at the interface is mostly due to the immediate oxidation of a Ge wafer in the air, even after the HF treatment [[39](#_ENREF_39), [40](#_ENREF_40)]. When the Si film is in contact with Ge, the Ge–O bonds can be replaced by Si–O bonds even at room temperature [[42](#_ENREF_42)]. More bond replacement can be triggered by high temperature annealing and the O peak location can be moved toward the Si side. Different from Si/Ge bonding with certain interface oxidation, an almost uniform O distribution across the whole cross section and thus no remarkable interface oxidation have been found in similar studies for Si/Si bonding when both the Si film and its bonded Si wafer are passivated with HF cleaning [[33](#_ENREF_33)].

Along the scanning direction indicated in Fig. 5b, the EDS line scan (Fig. 5c) shows the element distribution across the interface. The Si/Ge interface is suggested to be a layer of mixed SiOx and Ge [[39](#_ENREF_39)]. In such cases, the O concentration at the interface and interlayer thickness can be critical to the thermal transport across the interface. In analogy, electrical measurements across such junctions shows a dramatically reduced on-current when the interlayer thickness is increased from 3 nm to 3.5 nm after 673 K annealing [[39](#_ENREF_39)]. For thermal transport, reducing the interfacial requires minimized Ge surface oxidation during the fabrication process.

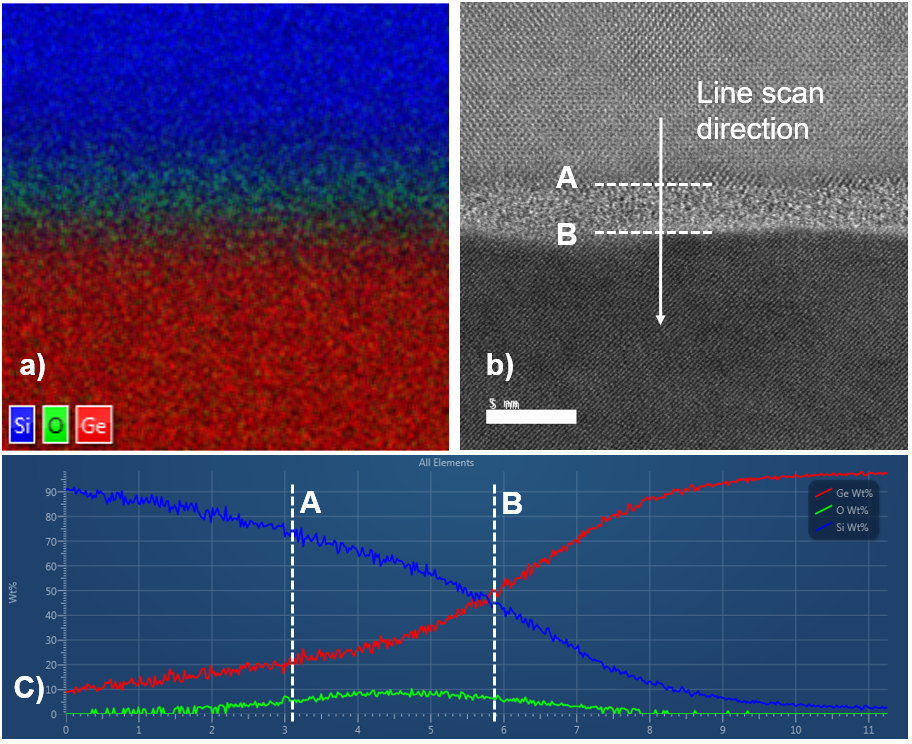


Figure 5. (a) Element mapping of the Si/Ge interface for the sample with a 12.6˚ twist angle. (b) SEM image of the element mapping area. (c) EDS line scan across the interface, along the A–B direction indicated by (b).

*3.3 Temperature-dependent of Si/Ge heterojunctions with varied twist angles*

Figure 6 shows the extracted interfacialfor Si/Ge bonding, with the error bars indicating the uncertainty described in Section 2.2. Weak dependence on the twist angle between the film and wafer is found here. In contrast, film-wafer bonding studies for an Si/Si interface show strong twist angle dependence for the interfacial , which is further correlated with the strain field on the interface [[33](#_ENREF_33)]. The measured values for Si/Ge bonding here are generally higher than those for Si/Si bonding, the latter of which ranges from 5.5×10-9 m2·K/W to 2.8×10-8 m2·K/W at 300 K. The contrast here suggests that the amorphous interlayer can be dominant for blocking the thermal transport. Without considering any oxidation, MD simulations suggest that the SiGe alloy interlayer functions as the major bottleneck for the interfacial thermal transport [[15](#_ENREF_15)]. For and interlayer thickness of 2.27 nm, of ~1.0×10-8 m2·K/W at 300 K is computed for Si/Ge bonding with a 0˚ twist angle. The higher values measured in this work are attributed to the slightly thicker interlayer and amorphous SiOx within the interlayer. In addition, the interdiffusion between Si and Ge extends beyond the <3 nm interlayer in Fig. 5c. These additional alloy regions are also resistive to thermal transport.

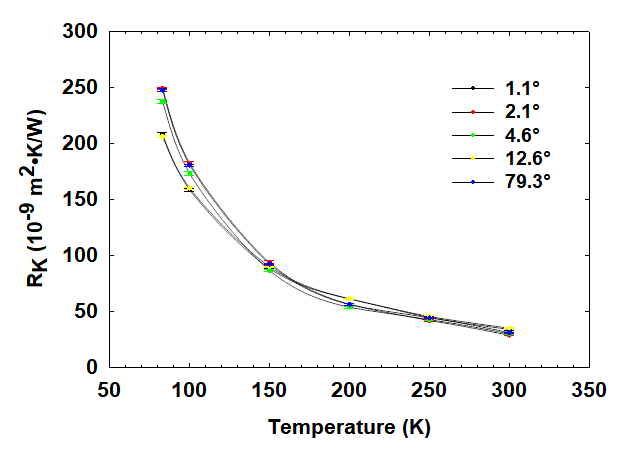


Figure 6.Temperature-dependent *RK* for representative samples.

**4. Conclusions**

Despite the wide use of Si/Ge bonding for device applications [[21](#_ENREF_21), [22](#_ENREF_22), [39](#_ENREF_39)], the corresponding thermal studies have been lacking. For nanocomposites formed by hot press, the Si/Ge interface formation under a high temperature is not well understood for their impact on interfacial thermal transport. In this study, the systematic interfacial thermal transport suggests that the alloying and oxidation within the interlayer play an important role in restricting the thermal transport, which is consistent with previous MD simulations [[15](#_ENREF_15)]. Although numerous studies have been carried out on the reduction with engineered heterostructure interfaces [[43](#_ENREF_43), [44](#_ENREF_44)], the interdiffusion between different materials during the interface formation and possible oxidation must be considered in real experiments. Particular attention should be paid to those interfaces formed under hot press, where interdiffusion is inevitable for heterostructures.

Acknowledgements

Qing Hao thanks the support from National Science Foundation CAREER Award (grant number CBET-1651840).

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